30-V MMIC POWER AMPLIFIER WITH NOVEL BIAS CIRCUITRY*

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Abstract

High-voltage power amplifiers allow more efficient DC power conditioning and distribution than is possible with low-voltage systems. Results are presented for the first fully monolithic High-Voltage FET amplifier, with on-chip power combining and novel bias circuitry. Output power greater than 2 W was obtained with 30-V drain bias at 11 GHz. A power-added efficiency of 34 percent was also achieved, which is believed to be the best reported for such amplifiers.

INTRODUCTION

Present field-effect transistor (FET) power amplifiers typically require a bias voltage of 6 to 10 V. If amplifiers with the same efficiency could be made to operate at a much higher voltage, total system efficiency would be improved. This improvement would be attained through reduced ohmic loss in the DC power distribution network in systems such as phased-array antennas, and through improved efficiency in any required DC-to-DC power converter, such as is normally used to reduce satellite bus voltage from approximately 30 V to the lower voltage needed for solid-state power amplifiers (SSPAs).

In phased-array applications that require a large number of active devices, the I^2R loss in the DC distribution network is quite high. Raising the DC voltage by a factor of 4 will reduce ohmic loss by a factor of 16, which can be significant, even for low-loss distribution networks. Many systems have available a voltage source much higher than that required by conventional SSPAs. Specifically, satellites routinely have prime power available at 28 to 40 V. A DC-to-DC converter (with typically 85-percent efficiency) is required in order to drop the voltage to a level acceptable to the SSPA. Figure 1 illustrates the potential DC power savings in a total system. The conventional system shown requires 1,200 W, while the high-voltage system needs only 1,001 W, a savings of 20 percent. (If the satellite bus is not regulated, a simple and efficient series regulator may be used.) The mass can also be considerably reduced by elimination of the converter and use of lighter weight cable to distribute power to the SSPAs.

Previously, two-cell High-Voltage FET (HVFET) microwave integrated circuit (MIC) amplifiers (1), and two- and four-cell monolithic microwave integrated circuit (MMIC) amplifiers with external RF power-combining and biasing networks at an output power of 0.8 W (2), have been demonstrated. This paper discusses the design, fabrication, and measurement of a 2-W, Ku-band, fully monolithic HVFET amplifier with on-chip power combining and gate bias circuitry.

Earlier amplifiers used either separate voltage supplies for each gate, or a simple voltage divider between drain and ground. Using separate DC power supplies provides good amplifier performance, but also increases total system cost and bulk. Use of a resistive voltage divider will resolve this problem; however, the resistance values must be high to avoid wasting DC power. When a class AB amplifier reaches saturated output power, it will draw gate current. This current passes through the resistive voltage divider and causes the gate bias voltage to shift toward class A operation, thus limiting efficiency. The present amplifier includes on-chip constant-voltage sources to allow highly efficient operation with a minimum number of external power supplies.

DEVICE AND CIRCUIT DESIGN

The HVFET is composed of individual FET "cells," connected in DC series and RF parallel. Each cell contains a conventional FET with its source connected to a capacitor to ground, as well as an inductor connected from the source

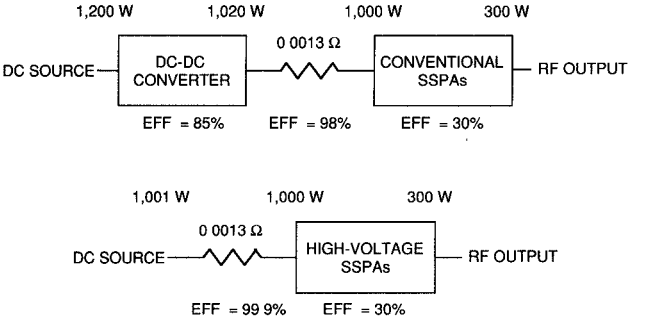

Figure 1. Comparison of Power Budgets With Conventional and High-Voltage SSPAs

* This paper is based on work performed at COMSAT Laboratories under the sponsorship of the Communications Satellite Corporation.

to the drain of the next cell for RF isolation. The structure, geometry, and material parameters of the FET device were optimized for the high-voltage implementation by using an in-house device modeling program. Nominal gate length was 0.5 μm. Gate width was 1.6 mm for each of four cells. Several advantages are realized by dividing the gate width into smaller cells. The smaller FET cells have higher impedance and so can be more efficiently matched for a given bandwidth. Because the total gate width is the same, device process yields are expected to be the same. Furthermore, since the generated heat is distributed across several HVFET cells, lower channel temperatures and improved reliability can also be expected.

The gate-bias circuitry must provide a relatively constant gate voltage over the expected range of gate current under large-signal class AB operation. A small 40-μm FET was configured to operate in the source-follower mode, with the reference voltage coming from a resistive dividing network connected between the drain and the last gate. This network may use large resistances to conserve power without causing the gate bias voltages to shift as gate current is drawn. The resistor of the small FET (and its gate width) were designed to provide a nearly constant voltage over the range of gate current that the larger power FET might draw during large-signal operation. For best efficiency, the quiescent current of the small FET should be only as much as will be drawn by the amplifier under large-signal conditions. Figure 2 shows the results of a time-domain circuit simulation of the gate bias circuitry, performed using the SPICE program. The voltage remains relatively constant over ±2 mA of gate current, which represents the gate current of the larger power FET. The reference voltage was stepped to simulate changes in amplifier bias.

Each HVFET cell has input and output impedance comparable to a conventional FET at the frequency of operation. The RF circuitry was designed, using an in-house load-pull CAD program, to achieve the best gain and power over satellite down-link bands from 10.95 to 12.2 GHz. The second harmonic is terminated at the device drain to improve amplifier power-added efficiency (3). The source capacitor was chosen to be sufficiently large to provide a good electrical short at the frequency of operation, and enough below that frequency for the R-C stabilization network to begin to roll off. An R-C circuit in the gate bias network provides bias voltage through a resistor and ensures stable operation below the frequency of operation. The resistor was designed with a very low value and was realized using thin capacitor base-plate metal. Other resistors were realized as n/n^+ mesa resistors. At very low frequencies, the source capacitor acts like an open circuit and the FET source "sees" the output resistance of the next FET cell, which provides negative feedback and stability down to DC. Figure 3 shows the circuit topology of the entire amplifier.

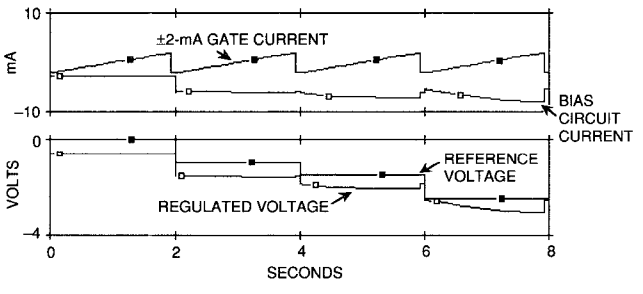

Figure 2. Simulated DC Performance of Gate Bias Circuit

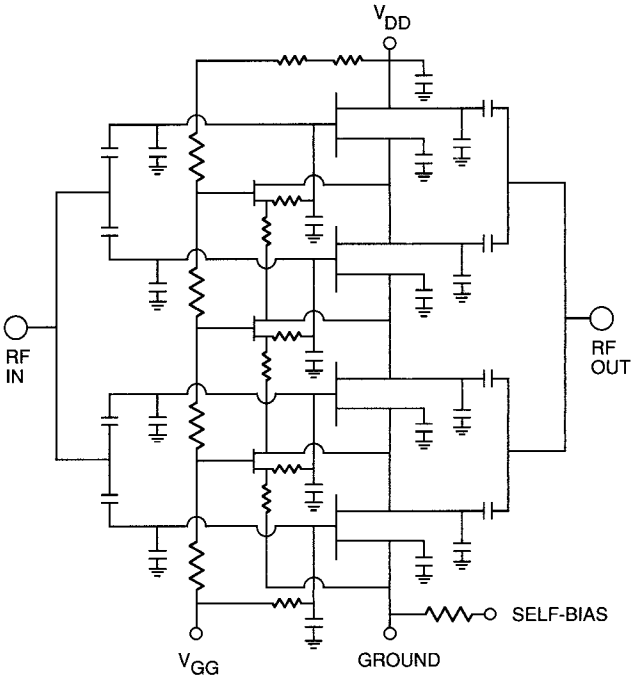

Figure 3. HVFET Amplifier Topology

MMIC FABRICATION

The amplifiers were fabricated using COMSAT's power FET process (4) on molecular beam epitaxy (MBE) gallium arsenide (GaAs) material. A super-lattice buffer layer was used to impede the out-diffusion of defects from the semi-insulating substrate into the active channel. Optical photolithography and direct e-beam written gates were employed, and via-hole technology was used to provide low-inductance grounding for the bypass capacitors. A double-recess gate process was used to allow the generation of high electric field potential in the gate channel region without premature avalanche breakdown. Figure 4 is a photograph of the HVFET MMIC.

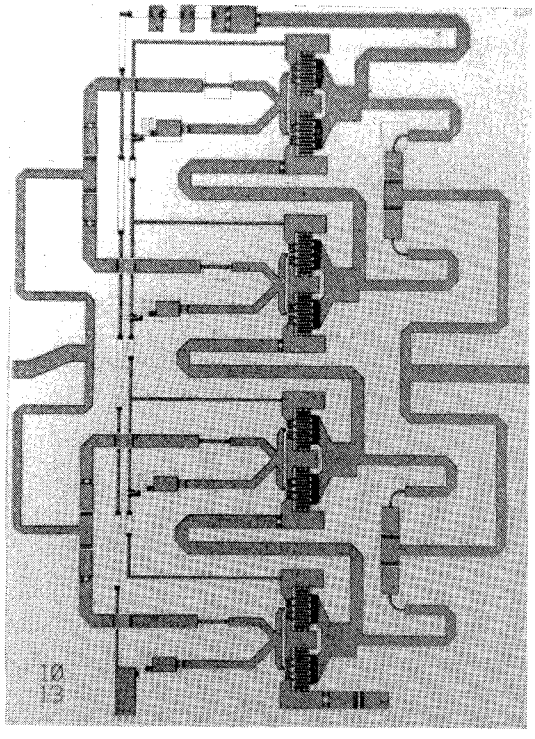

Figure 4. HVFET MMIC (Die size = 3.075 x 4.175 mm)

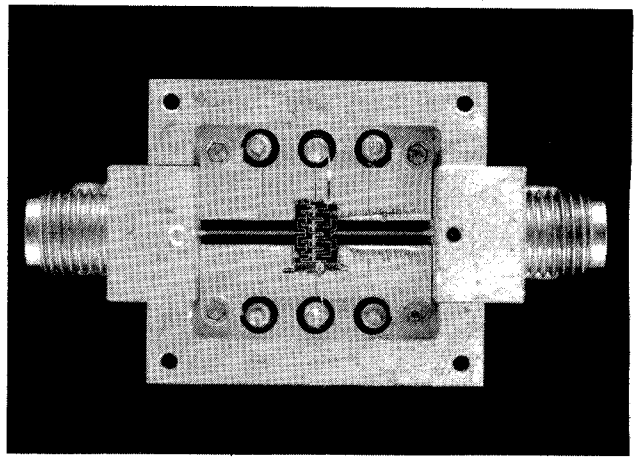

Figure 5. Assembled HVFET Amplifier

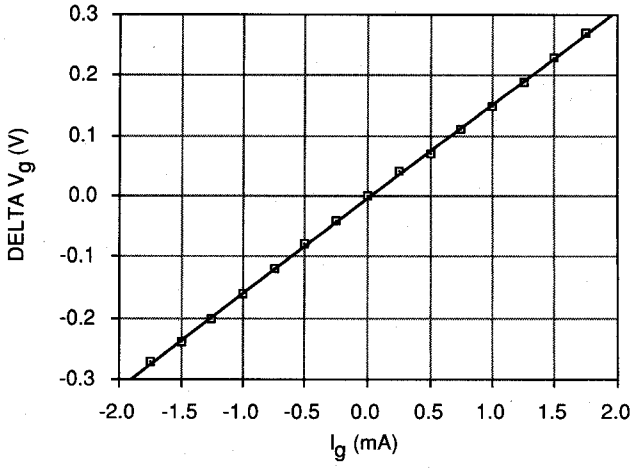

Figure 6. Measured Change in Gate Voltage vs Gate Current

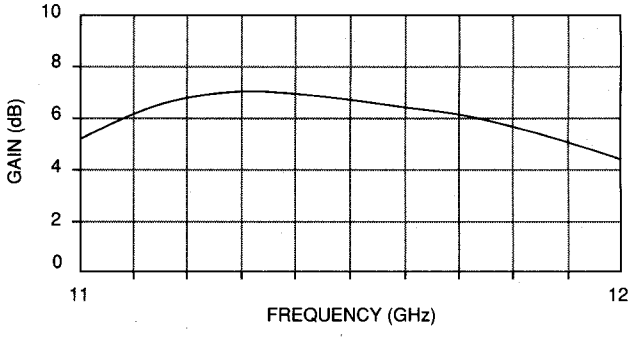

Figure 7. Small-Signal Gain Response of MMIC Amplifier at 30-V Bias

MEASURED RESULTS

Figure 5 shows a packaged MMIC HVFET amplifier. A drain voltage of 30 V was used to bias the amplifiers, with the bottom FET gate biased at -1.8 V. To verify the operation of the gate bias circuitry, the gate voltage of one of the FETs was probed and a small amount of current was injected to simulate the breakdown of the large power FET. Figure 6 is a plot of this measurement. The gate voltage, V_g, remained constant within 0.25 V of the original value as the gate current, I_g, was varied to ±1.6 mA. These results demonstrate that the bias circuit is performing as designed and that the bias voltage will be constant, even under large-signal class AB operation of the amplifier.

The small-signal gain response of the four-cell HVFET power amplifier from 11 to 12 GHz at a 30-V drain bias is depicted in Figure 7. Figure 8 shows the output power and power-added efficiency at 11 GHz plotted vs input power. Saturated output power of 2.3 W was achieved. Figure 9 shows the amplifier operated for best power-added efficiency at 11 GHz; 34 percent was attained.

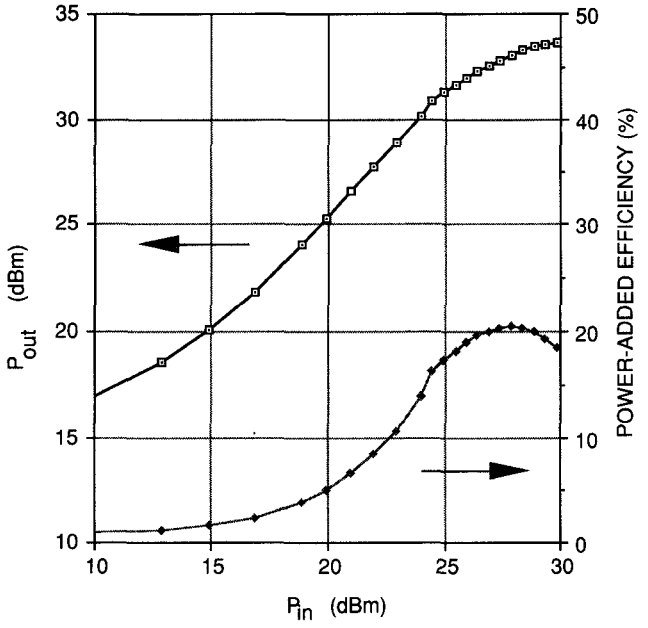

Figure 8. Output Power and Power-Added Efficiency vs Input Power

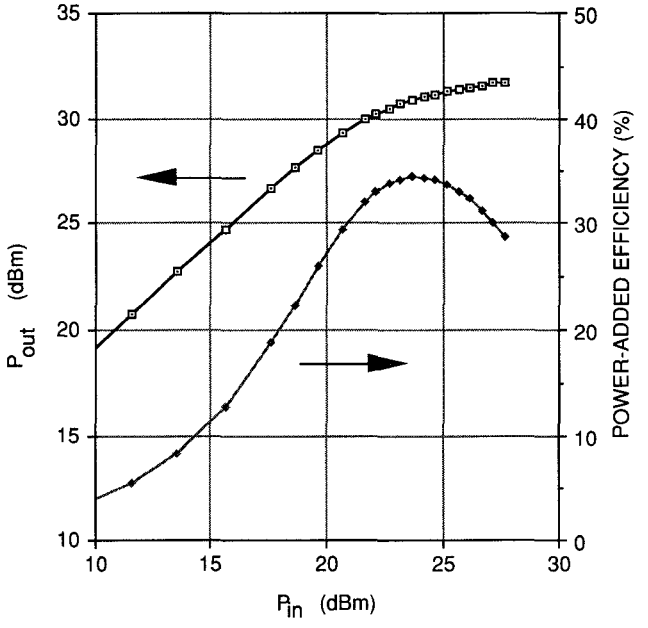

Figure 9. Amplifier Operated for Best Power-Added Efficiency

CONCLUSIONS

Successful operation of Ku-band, fully monolithic HVFET amplifiers at 30 V, with on-chip constant-voltage gate bias circuitry biased near satellite bus voltages, has been demonstrated for the first time. The bias circuitry developed here allows the high-voltage amplifier to be biased for class AB operation. This will lead to improved DC-to-RF conversion efficiency in satellite transponders by allowing the elimination of an electronic power converter, or its replacement by a simple voltage regulator. The techniques developed are also suitable for other applications that have limited prime power budgets, such as active phased-array antennas.

ACKNOWLEDGMENTS

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